REMARKS/ARGUMENTS

In response to the Office Action mailed June 27, 2005, Applicants amend their application and request reconsideration. Non-elected claims 1 and 2 are cancelled and elected claims 3-12 are replaced by new claims 13-24. Accordingly, claims 13-24 are now pending.

The invention, as it pertains to the elected method claims, concerns a method of manufacturing a silicon carbide vertical MOSFET. Figure 1 illustrates such a structure and similar structures are known in the prior art. In that structure, as shown in cross-section in the embodiment of Figure 1, a substrate 7 has grown upon it an epitaxial layer of SiC. An insulating film 2 on the exposed surface of the grown layer is covered by an oxide 2 upon which a gate 1 is disposed. On that same surface of the grown layer, a source electrode 3 is present. Beneath the source electrode, within the grown layer, is a source region formed by ion implantation in the grown layer. The source region 4 is within a base region 5. That base region 5 is also produced by ion implantation and has a conductivity type opposite the conductivity type of the source region, the epitaxial layer, and the substrate 7. A drain electrode 8 is disposed on the opposite side of the substrate 7 from the epitaxial layer 6. The epitaxial layer is referred to, when the source and base regions are present, as the drift region. Charge carriers flow from the source region through the base region 5 to reach the drift region where, under the influence of an electric field, they drift to the drain electrode 8. The potential on the gate electrode 1 controls the flow of charge carriers from the source region through the base region. These transistors have extremely high withstand voltages, the example cited in the patent application having a withstand voltage of 1,200 volts. These devices are used in inverters and other applications employing high voltages.

Accordingly, with reference to Figure 1, it can be seen that when current flows in the transistor of Figure 1, the current principally flows in a direction that is nearly vertical in that figure, in contrast to silicon MOSFETs in which the current generally flows parallel to the substrate, i.e., horizontally. Further, as shown in Figure 1, there appear to be two source regions 4 and two base regions 5. In actuality, there is a single such source region and a single such base region because, in plan view, as known to those of skill in the art, the source and base regions surround the part of the drift region that projects toward and contacts the oxide layer 2. In the simplest such structure, both the source region and the base region have

a generally annular configuration. Thus, several characteristics of the vertical transistor, such as the breakdown voltage, depend upon the minimum thickness of the base region 5, a spacing that may vary, as shown in Figure 2, when the interface of the base region and drift region is oblique to the surface of the SiC epitaxial layer 6.

The characteristics of SiC vertical MOSFETs significantly depend upon the configurations of the source and base regions. The invention provides several methods of achieving desired device structures having electrical characteristics that make the devices particularly useful. With the high voltages that are experienced between the source and base regions, an important consideration is "punch-through", i.e., the breakdown of the pn junctions between the base and source regions and between the base and drift regions. The maximum withstand voltage, i.e., non-breakdown voltage, depends upon the charge carrier concentrations in each of these three regions as well as the separation of the regions. For example, that separation may be measured in terms of the channel length which is the length along the surface of the epitaxial layer between the drift region and the source region. Or, the separation may be the minimum thickness of the source region, i.e., the minimum distance between the source-base region interface and the base-drift region interface. Of course, as the channel length or minimum source region thickness is increased in order to increase the withstand voltage, the resistance of the channel also increases. In other words, in determining the channel length there is a trade-off relationship between the withstand voltage for a device of a fixed size and the resistance which is controlled by the width of the drift region as measured between the symmetrical parts of the base region.

The newly supplied method claims include four independent claims, claims 13, 17, 20, and 22. These claims are related to and supported by original claims 4, 5, 8, and 9, respectively. The methods according to independent claims 13 and 17 describe the use of an ion implantation mask that has, in cross-section, a tapered shape like the mask 9 illustrated in Figures 10, 20, and 22 of the patent application. Those figures and the description concerning those figures support claims 13-20.

As explained in the patent application, the angle of the interface between the drift region and the base region has a critical influence on the withstand voltage of the device as well as the resistance of the device. It is critical, in order to avoid breakdown of the device, i.e., punch-through, that the angle be most preferably in a range of 30° to 45°. This angle is

illustrated as angle θ, for example, in Figures 5, 6, 9, and 11 of the patent application. In order to achieve that range of taper angle of the base region using a tapered ion implantation mask, the side surfaces of the ion implantation mask must form an angle, within a specified range, with the surface of the epitaxial layer of silicon carbide. This relationship is explained in the patent application with respect to, for example, Figures 10-12 of the patent application. That description, at pages 12-14 of the patent application provides support for the angular range of the side surfaces of a tapered mask of silicon carbide, according to claim 13, and the similar ranges for a tapered mask of silicon dioxide as described in independent claim 17. Because the implantation penetration characteristics of silicon dioxide are different from those of silicon carbide, different side surface orientations of the tapered ion implantation mask are required to produce the same results with masks of different materials.

Dependent claims 14-16 and 18-20 are clearly supported by the application as filed. The implantation of the first and second ions at different angular orientations is described in the patent application with respect to the use of a tapered mask at least in connection with Figure 20. The parallel arrangement of interfaces of both the source and drain regions is described for all embodiments employing a tapered mask, and illustrated in Figures 10, 20, and 22. Simultaneously implantation of both the first and second ions is described in the patent application at least at page 18, lines 7-9.

Independent claims 21 and 23 describe another method of manufacturing a vertical MSFOT of silicon carbide using a mask that does not include tapered sides. Examples of such masks are illustrated in Figures 14 and 21 of the patent application. Different considerations apply in using such a mask since the varying thickness of the tapered parts of the mask used in the process of claims 13 and 17 are missing. The difference in direction of ion implantation and the limitations on the angles of ion implantation in use of this kind of mask in order to achieve the critical result of the invention are described in the patent application with regard to embodiment 3 at pages 14-18. Those pages provide direct support for each of independent claims 21 and 23. Independent claim 21 describes a process employing a silicon carbide mask whereas independent claim 23 describes a process employing a silicon dioxide mask. Again, the range of angles of ion implantation in these two processes are different because of the different penetration characteristics of the mask materials. The critical limitation for achieving a desired device characteristic is expressed in claim 21 in terms of channel length. In claim 23, that critical dimension is the minimum

punch-through length, Lp, the base region minimum thickness. Dependent claim 22 and 24 are supported by the same disclosure of the patent application that supports claims 16 and 20.

Examined claims 4 and 8 were rejected as indefinite as referring to a material having an ion implantation characteristic the same as silicon carbide without identifying the material. The claims now presented do not include similar language and, where the same intent is present, the material is specified as silicon carbide. Silicon carbide must have the same characteristics as itself so that the rejection of claims 4 and 8 as indefinite is no longer applicable.

Examined claims 3, 6, 7, and 10-12 were rejected as anticipated by Takeuchi (JP 11-274173).[1] This rejection is no longer pertinent because no claim corresponding to any of the claims rejected as anticipated is pending in the patent application.

Claims 5 and 9 were apparently rejected as obvious over Takeuchi. The Office Action is defective as to this point since it appears that clam 9 was rejected only by inference. There was no prior art rejection explicitly stated with regard to examined claims 4 and 8. All rejections, whatever they may be, with regard to Takeuchi, are respectfully traversed as to the claims now pending.

Careful attention has been given to Takeuchi. There appears to be no English language counterpart of that publication. However, a computer-generated English language translation of that publication has been consulted. That translation is available from the JPO website.

As perhaps already conceded in the Office Action, although not clear from it, while Takeuchi is certainly pertinent prior art, Takeuchi does not describe any process of making an SiC vertical MOS transistor employing an ion implantation mask of silicon carbide. Further, there is no suggestion for use of such a mask. The only masks employed by Takeuchi are so-called low temperature oxide masks, namely silicon dioxide or, perhaps, other oxides of silicon. Therefore, it is apparent that all of claims 13-16, 20, and 21 are patentable over Takeuchi. Even if the Examiner were to take the view that use of silicon carbide as an ion implantation mask is suggested by Takeuchi, a position that would be incorrect, Takeuchi fails to disclose or suggest other limitations of claims 13-16, 20, and 21, such as the specified angular ranges of implantation. Applicants reserve the right to submit additional arguments,

[1] The Examiner referred to the first-named inventor by his given name rather than his family name. The family name is employed here.

distinguishing these claims further from Takeuchi, if the rejection should be maintained. However, based upon the Office Action of June 27, 2005, it is apparent that these two groups of claims, claims 13-15, 20, and 21, are clearly patentable over Takeuchi.

Claims 17-20, 23, and 24 are clearly patentable over Takeuchi. Applicants agree that Takeuchi describes methods of manufacturing SiC vertical MOSFETs employing ion implantation masks of silicon dioxide. The mask 20 illustrated in Figure 2(a) of Takeuchi has a tapered shape in cross-section and the mask 25 illustrated in Figure 8(a) of Takeuchi includes side surfaces that are essentially perpendicular to the surface of the epitaxial layer 2. However, Takeuchi never describes, with respect to the tapered mask, any reason to taper the mask at any particular angle. Takeuchi only mentions the possibility of forming such tapered side surfaces by isotropic etching. See paragraph [0041] of Takeuchi. Since silicon dioxide is not a crystalline material, the angles of the side surfaces of the tapered mask are completely arbitrary angles, depending upon the etchant used, how the silicon dioxide layer forming the mask is, itself, masked, the duration of the etching, and other variables. Clearly, Takeuchi neither discloses nor suggests any criticality in establishing the angle of the side surface of the tapered mask. Therefore, Takeuchi cannot possibly suggest any of claims 17-20.

Takeuchi, at paragraphs [0060]-[0065], describes the process illustrated in his Figures 8(a)-8(c). Although this process employs a silicon dioxide mask with side surfaces perpendicular to the surface of the epitaxial layer 2, and two ion implantation steps, one at an angle and one perpendicular to the surface of the epitaxial layer 2, there is absolutely no discussion in Takeuchi concerning specific angles or ranges of angles of ion implantation or why specific angles should be employed. Again, it is apparent that Takeuchi has failed to comprehend, disclose, or suggest the criticality of the ion implantation ranges and their relationship to the material of the mask as described in independent claim 23. Accordingly, claim 23 and its dependent claim 24 are patentably distinct from the disclosure of Takeuchi.

For the foregoing reasons, all claims now pending are clearly patentable over Takeuchi. Upon reconsideration, claims 13-24 should be allowed.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

Date: Sept 23, 2005
JAW:ves